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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,831	07/21/2003	Stephen W. Kiss	42P7576D	6571

8791 7590 07/27/2004

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,831	KISS ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030721*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 10, in line 23, "T12 **395**" is not shown in any figure. Examiner suggests deleting "395".

On page 11, in lines 8, 9 and 11, "T1 360" should read "T1 390".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 13-20 are rejected under 35 U.S.C. 102(e) as being anticipated by **Maloney** (6,269,199 B1).

Regarding claims 13, 16 and 17:

Maloney discloses (in Figs. 6A-6B and Col. 7, beginning on line 53) a method of making a symmetric transistor device comprising: depositing first conductive layer 402 (comprising polysilicon, note Col. 5, line 23, i.e., gate 204 is specified to be polysilicon), the first conductive layer forming an even number of transistor legs (i.e., six legs), laid out in an intersecting tic-tac-toe pattern, forming a bilaterally symmetric base; doping the substrate to form source and drain regions 404; and forming a plurality of transistors defined by a portion of a leg forming a gate and the source and drain areas on either side of the leg forming a source and drain (note Fig. 6B and Col. 8, lines 10-12, i.e., source/drains regions are formed in openings of the "gate grid 402". Therefore, these claims are anticipated.

Regarding claim 14:

Maloney discloses the gate is separated from the channel/substrate by a gate oxide layer (note Fig. 6B, Fig. 3; Col. 5, lines 56-57), wherein the gate oxide would be silicon dioxide (Note Col. 13, line 8, wherein Maloney specifies oxide to be silicon dioxide). Therefore, the gate oxide would silicon dioxide that would inherently be deposited prior to depositing the first conductive layer, since the gate oxide must be located between the substrate and the first conductive layer. Therefore, Maloney anticipates this claim.

Regarding claim 15:

Maloney discloses the source and drain regions are formed in the openings of the gate grid (note again, Col. 8, lines 10-12); therefore, the gate grid at very least serves as a diffusion

plate used for doping, wherein the gate-grid diffusion plate forms undoped areas at intersections of the transistor legs, i.e., regions covered by the gate grid remain undoped, e.g., note the channel region directly beneath the transistor gate 402 (in Fig. 6B). Therefore, Maloney anticipates this claim.

Regarding claim 18:

Maloney discloses (in Col. 8, lines 27-33) conductive interconnections (i.e., smooth silicide) between the source and drain areas to form a circuit.

Regarding claim 19:

Maloney discloses adjacent legs 402 (i.e., adjacent transistors) share source/drain regions (note Fig. 6B); therefore, the transistors formed by the three vertical legs will be oriented along a first axis, and the transistors formed by the three horizontal legs will be oriented along a second axis orthogonal to the first axis. Accordingly, half of the transistors are oriented along the first axis and the other half is oriented along the second axis. Therefore, Maloney anticipates this claim.

Regarding claim 20:

Maloney discloses (in Col. 8, lines 12-14) the gate electrode area and the source drain are approximately equal, i.e., the transistor structure is symmetrical. The minimum drawn W/L must be used for each transistor leg since the transistor structure is symmetrical. Therefore, Maloney anticipates this claim.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 are cited to show tic-tac-toe patterns used in two-level poly/metallization transistor structures, processes for doping source drain regions utilizing a "gate grid" as a diffusion plate, etc.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Fri (6AM-2PM EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

July 26, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800